**Amendments to the Specification:**

Please replace the entire paragraph [0003] on page 1 with new paragraph [0003] following:

[0003] Traditionally, the design of commodity [[of]] Dynamic Random Access Memory (DRAM) devices [[is]] has been more focused on achieving low cost-per-bit through high aggregate bit density than on achieving higher memory performance. The reason for this is that the cell capacity of a two dimensional memory array increases quadratically with scaling, while the overhead area of bit line sense amplifiers, word line drivers, and row address (or x-address) and column address (or y-address) decoders increase linearly with scaling. Therefore, the design emphasis [[focus]] on memory density has resulted in commodity DRAMs being designed having sub-arrays as large as practically possible, despite its strongly deleterious effect on the time needed to perform cell readout, bit line sensing, cell restoration and bit line equalization and precharge. As a result, the relatively low performance of traditional DRAM architectures as compared to Static Random Access Memory (SRAM) has generally limited its use to large capacity, high density, cost sensitive applications where performance is secondary.

Please replace the entire paragraph [0004] on page 1 with new paragraph [0004] following:

[0004] Furthermore, traditional DRAM architectures minimize the number of signal pins on memory devices by multiplexing address lines located between the row and column components of the address. As a result, the two dimensional nature of DRAM array organization has always been an inherent part of the interface between memory control or logic and DRAM memory devices.

Please replace the entire paragraph [0012] on page 3 with new paragraph [0012] following:

[0012] In accordance with an aspect of the present invention there is provided a method for accessing a dynamic random access memory (DRAM) having a plurality of memory storage elements located in rows and columns. A first memory access is initiated by providing a first

address signal indicative of the location of at least one memory storage element to be accessed. The first address signal is decoded to select a row and at least one column corresponding to the location of the at least one memory storage element. A word line corresponding to the selected row is enabled and a sense amplifier activated to latch data to or from the at least one selected column. The word line corresponding to the selected row is then disabled and the at least one selected column is precharged. A second memory access is initiated by providing a second address signal indicative of the location of at least one memory storage element to be accessed The second address signal is decoded to select a row and at least one column corresponding to the location of the at least one memory storage element, the second memory access commencing before the step of precharging the selected column has completed.

Please replace the entire paragraph [0031] on page 10 with new paragraph [0031] following:

[0031] Referring to Figures 9a and 9b, control circuit elements and data path elements for a sub-array according to one embodiment of the invention are illustrated generally by numeral 900. The general timing of operations on a selected sub-array is based on a single master timing reference signal, referred to as a word line timing pulse ($WTP_i$). A target address is input to an address register 902. An operation command is input to a register/decoder 903. Both the address register 902 and the register/decoder 903 are clocked by the synchronous interface clock signal CLK. The register/decoder 903 generates an internal READ, WRITE, or REFRESH ~~internal~~ command signal depending on the external command received.

Please replace the entire paragraph [0040] on page 12 and 13 with new paragraph [0040] following:

[0040] Referring once again to figure 10a, after a programmable preset delay D1, the word line timing pulse $WTP_i$ goes high, causing the bit line equalization signal BLEQ and the word line signal WL to go high. It should be noted that delays D1, D2, D3, D4 are all implemented using a novel delay circuit described in MOSAID co-pending application no. 09/616,973 and published as international application serial number WO 0203551A2 (herein incorporated by reference). After a programmable preset delay D2 from the rising edge of the clock signal, the RWACTIVE signal is asserted, causing the signal RSAMPCLK signal to go high. In response to the assertion of the word line signal WL, a voltage differential begins to develop across the bit line pair. After a combined delay D1 + D3, the sense amplifier power supply signals SAP, SAN are asserted, thereby amplifying the voltage differential across the bit line pair. After a combined delay D1 + D3 + D4, the local column select signal LSCL is asserted, thereby selecting a column from which data is to be transferred. In response to the assertion of the local column select signal LCSL, data is transferred from the selected column to an associated pair of data lines.

Please replace the entire paragraph [0041] on page 13 with new paragraph [0041] following:

[0041] It is important to note that each of the steps described above were initiated by self-timed signals derived from the master word line timing pulse [[$WTP_I$]] $WTP_i$ thereby allowing fine-tuning precision of the timing of each signal. It should also be noted that although the above description referred generically to one selected column and associated data line pair, one skilled in the art would appreciate that in fact multiple columns can be selected by a column select signal, each having associated data lines.

Please replace the entire paragraph [0045] on page 14 and 15 with new paragraph [0045] following:

[0045] For this reason, the self-timed nature of the present invention allows for a very tight control between the timing of the word line activation, the bit line sense amplifier activation, the

write driver activation and the column select activation. Specifically, the $WTP_i$ signal is self-timed from the clock signal CLK, through delay D1, gate 912 and flip/flop 910. The sense amplifiers [[and]] are then activated based on the self-timed circuit comprising delay D3 and gate 914. The same self-timed signal 916 generated by gate 914 is then used to drive delay D4 and gates 918 which are therefore self-timed from the activation of the sense amplifiers and will be activated precisely at the same time after the bit line sense amplifiers have been activated. Meanwhile, the write drivers 930 are also activated through self-timed circuitry formed by delay D2 and gate 920 and 928. In this manner, write drivers can more rapidly reverse an opposite phase logic state on bit lines to which they are writing to than in conventional DRAM implementations. Referring to figure 10b, a timing diagram for generating the $WTP_i$ signal is illustrated generally by numeral 1050. If the sub-array is active, or selected, the S input of the SR flip-flop 910 goes high. Consequently, the $WTP_i$ signal goes high and begins the sequence of control operations required for the command. The $WTP_i$ signal is reset to low at the next rising edge of the clock. This situation is illustrated as case 1. However, if the sub-array is inactive, or unselected, the S input to the SR flip-flop 910 remains low and, therefore, the $WTP_i$ signal remains low. This situation is illustrated as case 2 in figure 10b.

Please replace the entire paragraph [0046] on page 15 with new paragraph [0046] following:

[0046] Referring back to Figure 9, in relation to the pipelining of commands and the group select role, if a read operation is performed within a given sub-array group in cycle N, then its group select will be asserted during cycle N. The register 940 latches the group select ~~siganl~~ signal on the rising clock edge that separates clock periods N and N+1. The output of the register 940 controls the selection of the multiplexer 938 during clock period N+1.